~~ALU~~ MUX SELECTION EQUATIONS

MARK ARNOLD

$SR = (MANSW * (-EX) * CP0) + OPG2 * CP2$

$\cancel{PC = (JMS + OPG2) * CP0 + ISZ * CP2 + (A0 + F0 + F2 + A3)}$

$MB = (AND + TAD + ISZ) * CP0 + (F8 + F7)$

$CIN1 = DEP + EX$

$MA = JMP * CP0 + JMS * CP2 + CIN1 * CP6$

$AC = DCA * CP0 + OPG1 \cdot (CP2 + CP3)$

$M = F1 + F5 + F10$

$IR = F3$

$B42 = IR + M$

$B4 = B42 + SR$

$B2 = B42 + AC + MA$

$B1 = IR + AC + MB + SR$

ALU MODE SELECTION EQUATIONS

ALUS0 = (TAD + AND) * CP0

ALUS2 = OPG2 * CP2

ALUS1 = ALUS2 + AND * CP0

ALUS3 = ALUS0 + ALUS1

ALUM = ALUS3 + OPG1 * CP2

ALUCIN = A0 + F2 + F7 + (ISZ + OPG0) * CP0 + (ISZ + JMS) * CP2
+ OPG1 * CP3 + CIN1 * CP6

LOAD REGISTER EQUATIONS

LOADPC = A0 + F2 + (JMP + LDPC + OPG2 * IR8 @ (IR5 * ACN + IR6 * ACZ
+ IR7 * LINK1)) * CP0 + (MBZ * ISZ + JMS) * CP2

LOADMB = F1 + F6 + F8 + F10 + (ISZ + DCA + JMS + LDM + LDMB + DEP) * CP0

LOADMA = F0 + A4 + F5 + F9 + LDMA * CP0 + CIN1 * CP6

LOADAC = (AND + TAD + LDAC) * CP0 + (OPG1 * IR6 + OPG2 * IR9) * CP2
+ OPG1 * IR11 * CP3

LOADIR = F1 + LDIR * CP0

READ = F0 + F4 + F9 + A3

WRITE = F7 + (ISZ + DCA + JMS + LDM + DEP) * CP1

CLRWRITE = F8 + CP6

CLEARAC = OPG1 * IR4 * CP0 + (DCA + OPG2 * IR4) * CP1 + CLRP

CLEARL = OPG1 * IR5 * CP0

COMPL = OPG1 * IR7 * CP2 + COUT

I THINK THERE ARE
ERRORS UNDER-NEATH
FLOW CHART & THE
EQUATIONS DO NOT AGREE

CONNECTORS

C1

FRONT

1-3	4-5	6-7	8-9	10-11	12-13	14-15	16 ← → 28	29-30	31-32	33-34	35-38	39-40	41-42	43-44	45-46	47-48	49-50
GND	LINK	SR3	SR2	SR1	SR0	SRW	GND	SRX	SRY	SRZ	GND	SING INST	STOP	CLR	[illegible]	EX	DEP

BACK

100-99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51
CLOCK LOW	MA 3	M 3	MB 3	PC 3	IR 3	AC 3	MA 2	M 2	MB 2	PC 2	IR 2	AC 2	MA 1	M 1	MB 1	PC 1	IR 1	AC 1	MA 0	M 0	MB 0	PC 0	IR 0	AC 0	F 1	CLK LED	SD	PC L	IR L	LINK LED	F 2	RUN	S1	IE	MQ 1		F 4	MB L	S2	CIN	MQ 2	AC S0	F 8	MA L	S3	MQ 4	MQ 4	AC S1

C2

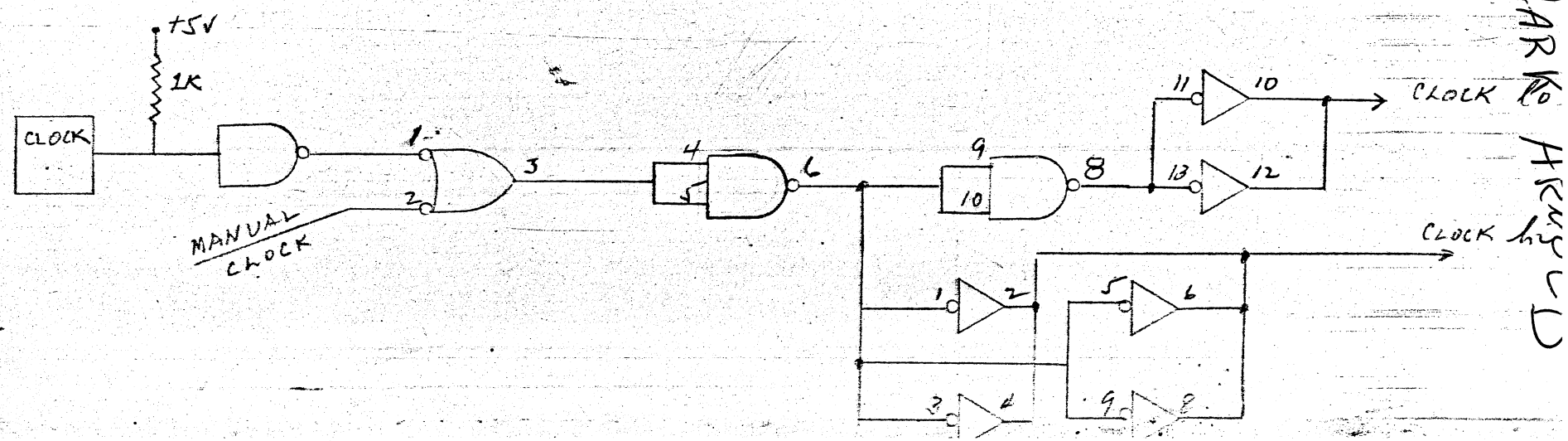
FRONT

1-2	3-4	5-6	7-8	9-10	11-12	13-16	17-20	21-24	25-29	30-31	32-33	34-35	36-37	38-39	40-41	42-43	44-45	46-47	48-50
LDMA	LDM	LDMB	LDPC	LDIR	LDAC	-5V	+5V	+12V	GND	SR 11	SR 10	GND	SR 9	SR 8	SR 7	SR 6	SR 5	SR 4	GND

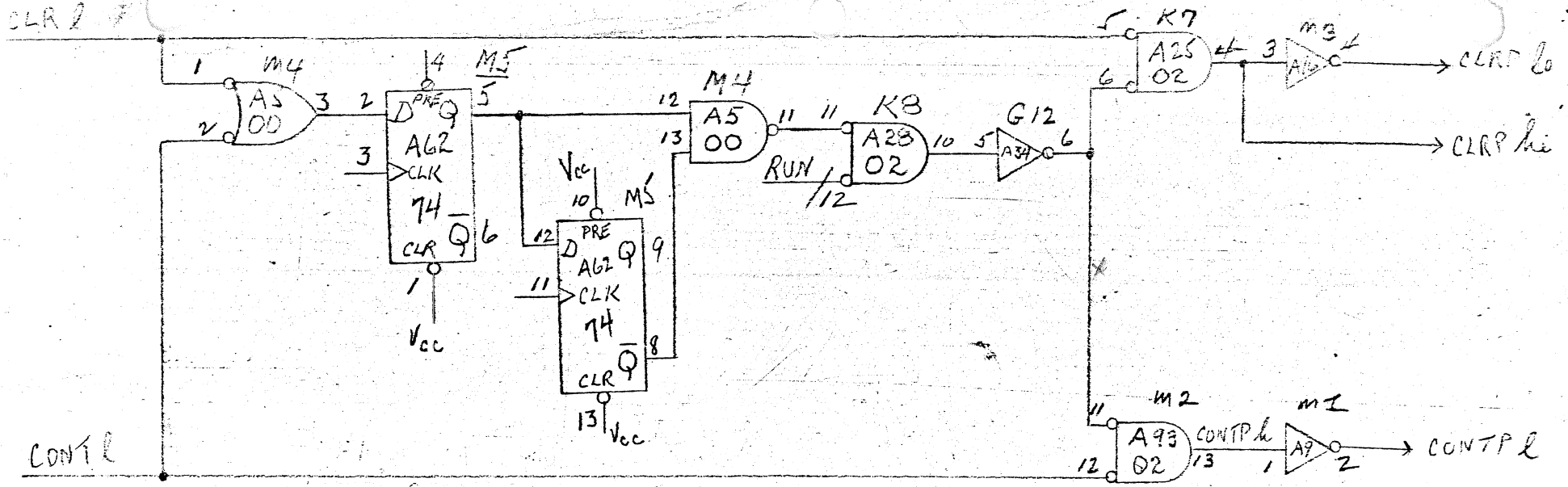
BACK

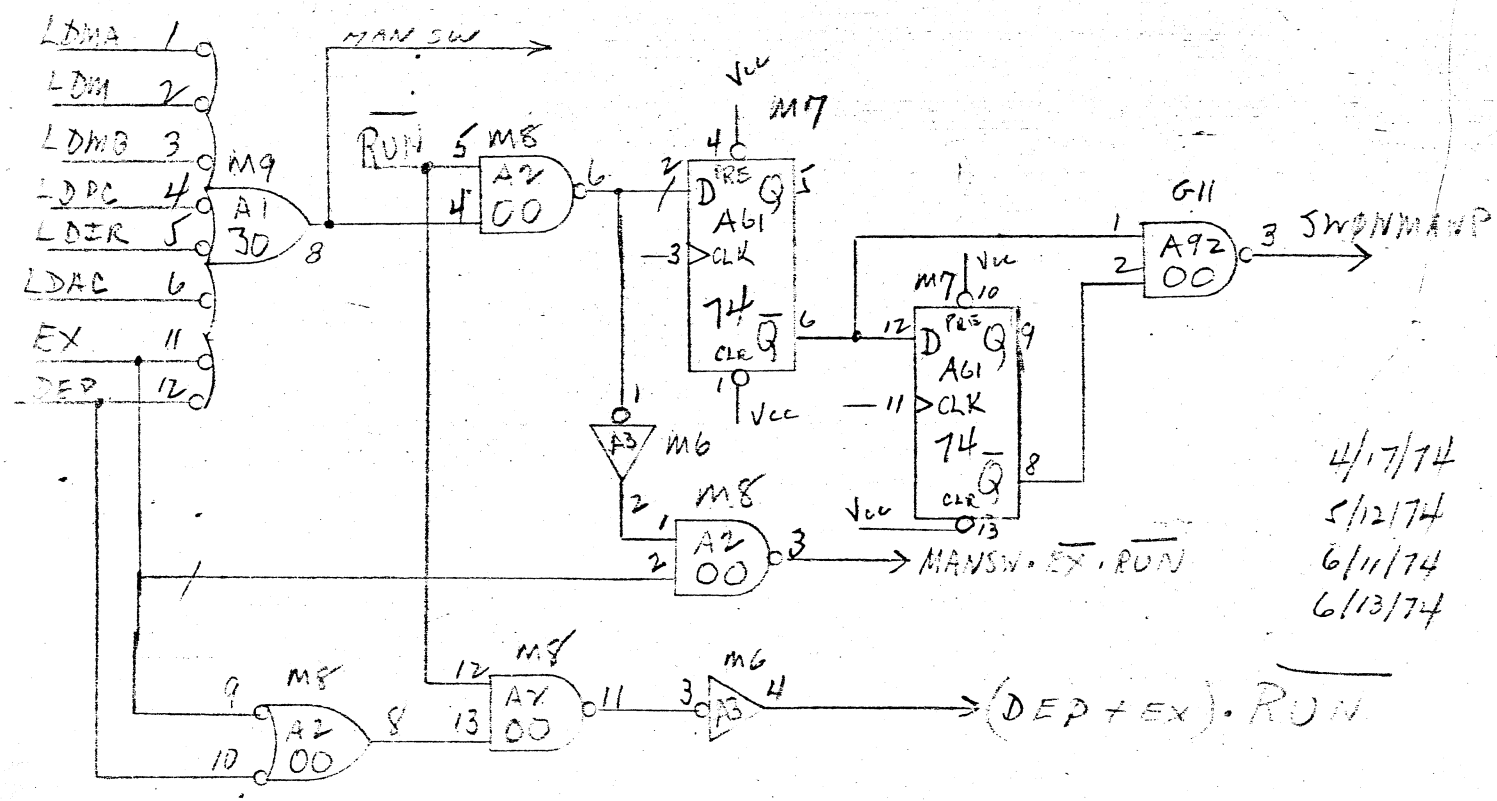
100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52-51
AC 11	IR 11	PC 11	MB 11	M 11	MA 11	AC 10	IR 10	PC 10	MB 10	M 10	MA 10	AC 9	IR 9	PC 9	MB 9	M 9	MA 9	AC 8	IR 8	PC 8	MB 8	M 8	MA 8	AC 7	IR 7	PC 7	MB 7	M 7	MA 7	AC 6	IR 6	PC 6	MB 6	M 6	MA 6	AC 5	IR 5	PC 5	MB 5	M 5	MA 5	AC 4	IR 4	PC 4	MQ 4	M 4	MA 4	CLOCK HIGH

CLOCK BOOST:

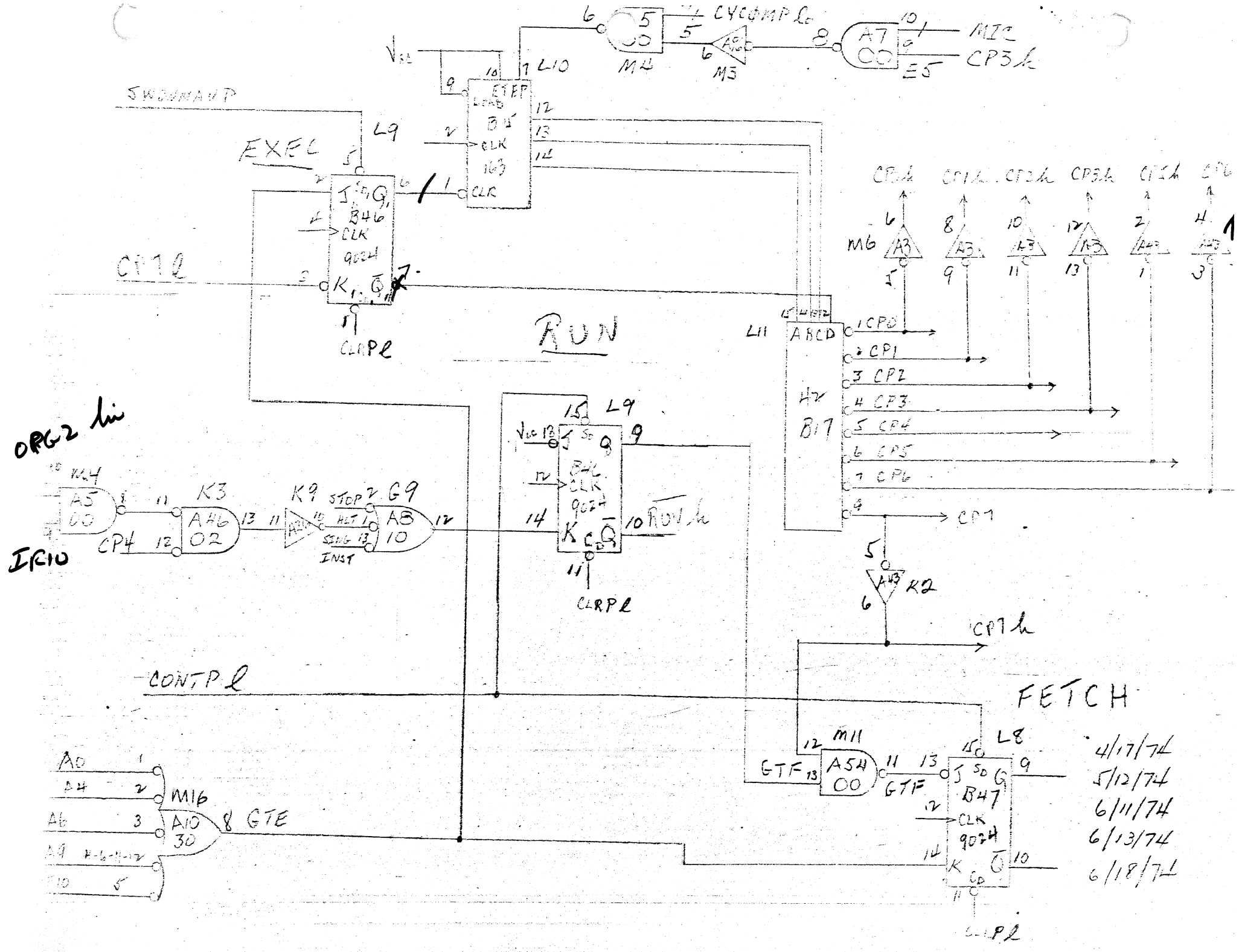


MARK Ko HRNYCH

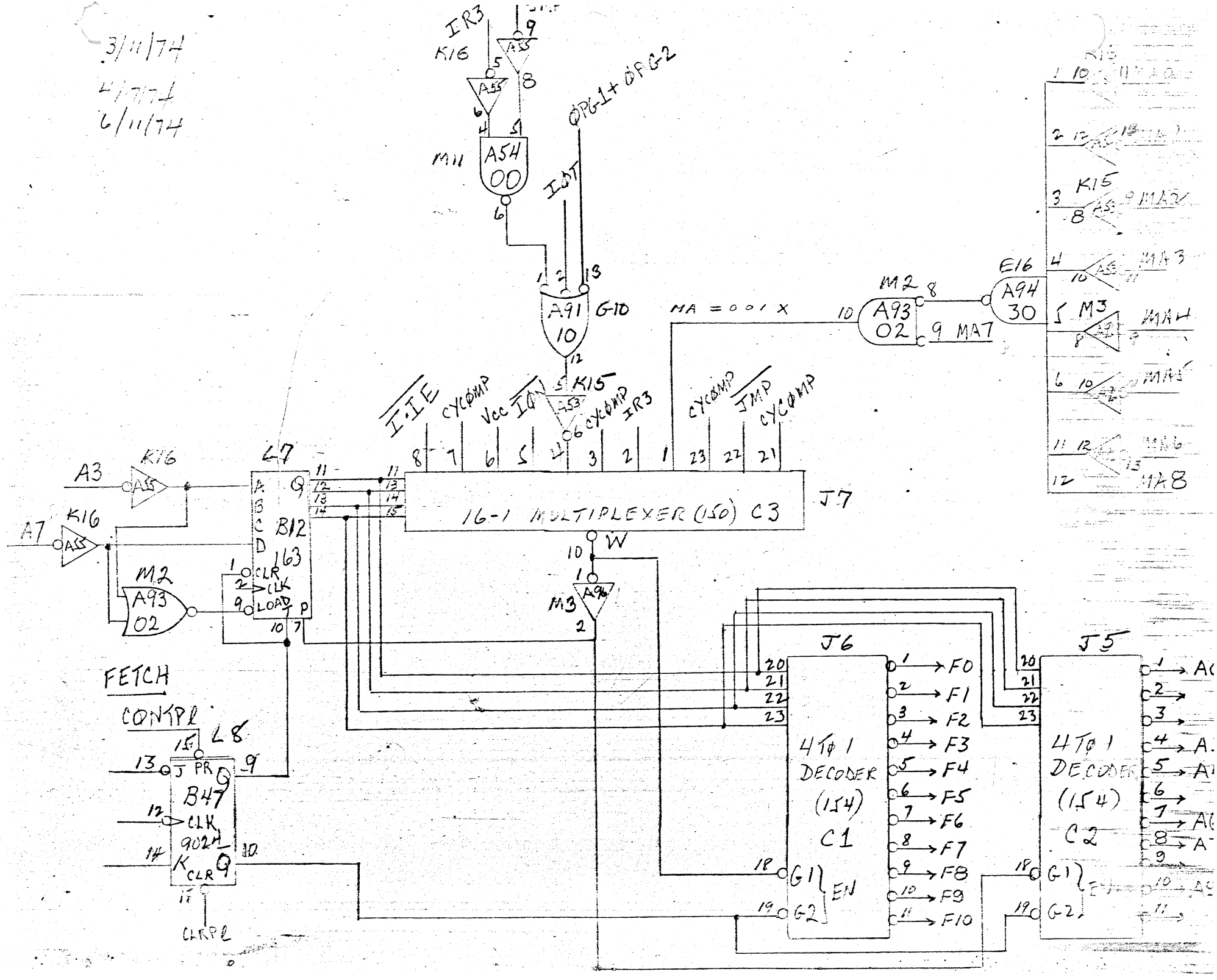


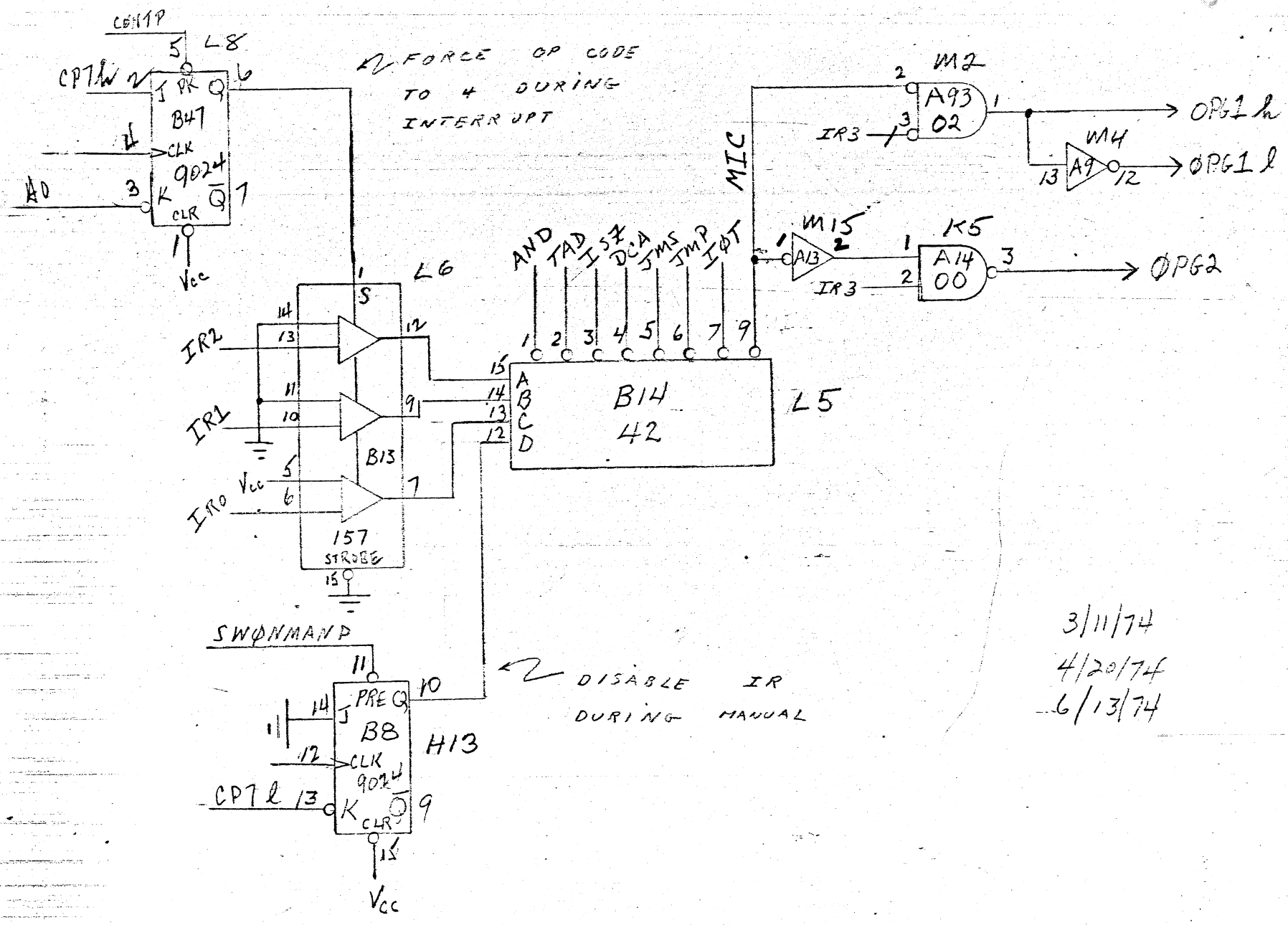


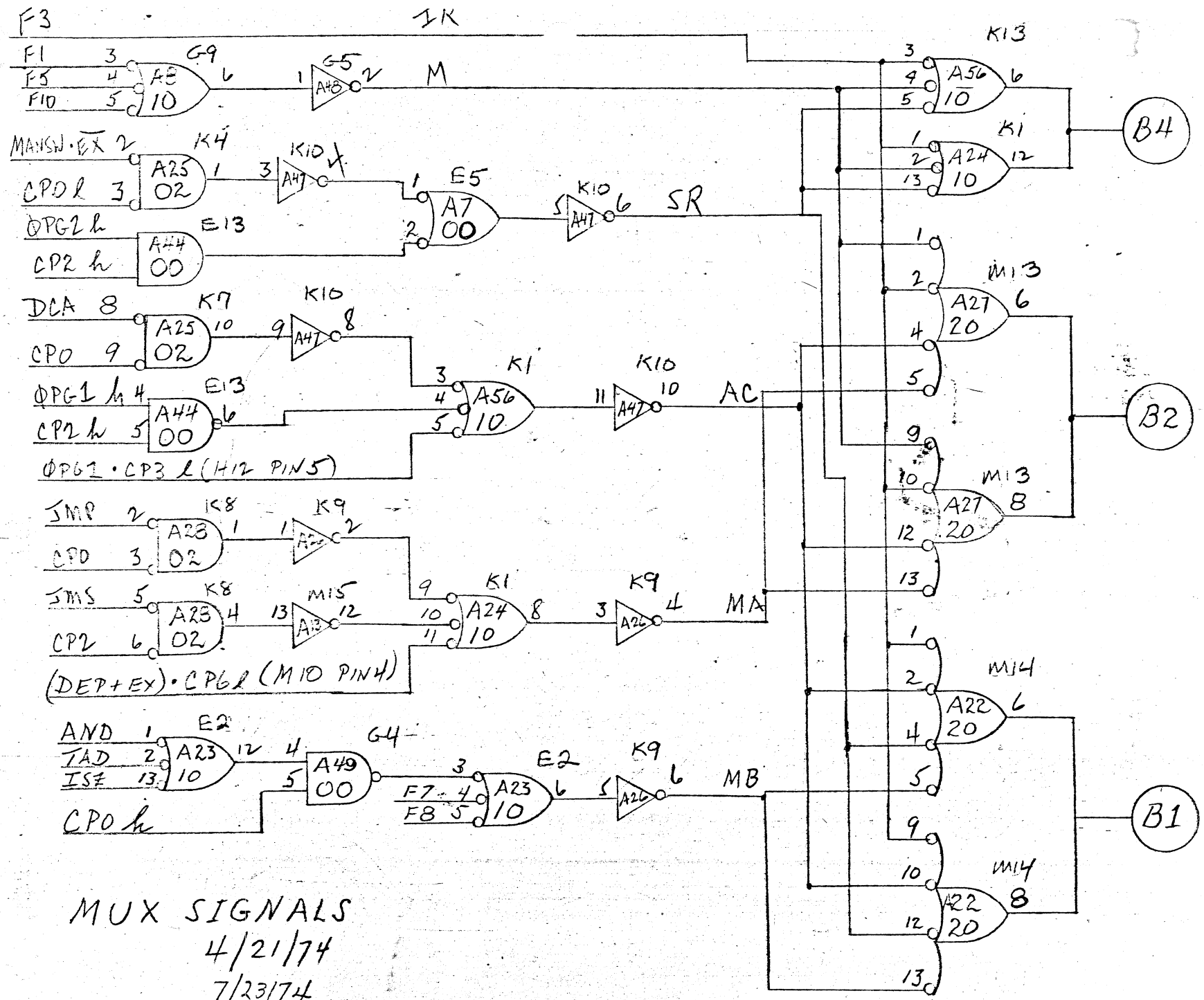
4/17/74
5/12/74
6/11/74
6/13/74


CYCOMPL
M2
M3
A7
E5
MIC
CP3h
L10
STEP
B45
CLK
163
CLR
SWRUNAND
EXEC
L9
J Q
B46
CLK
9024
K Q
CLRPl
CP7l
RUN
L11
ABCD
H2
B17
CP0
CP1
CP2
CP3
CP4
CP5
CP6
CP7
M6
A3
K2
CP7h
ORG2 hi
IC10
M4
A5
00
K3
A46
02
K9
STOP
HLT
SING
INST
G9
A8
10
L9
B46
RUNh
CONTPl
FETCH
M11
A54
00
GTF
L8
B47
M16
A10
30
GTE
A0
A4
A6
A9
A10
4/17/74
5/12/74
6/11/74
6/13/74
6/18/74

3/11/74
4/11/74
6/11/74

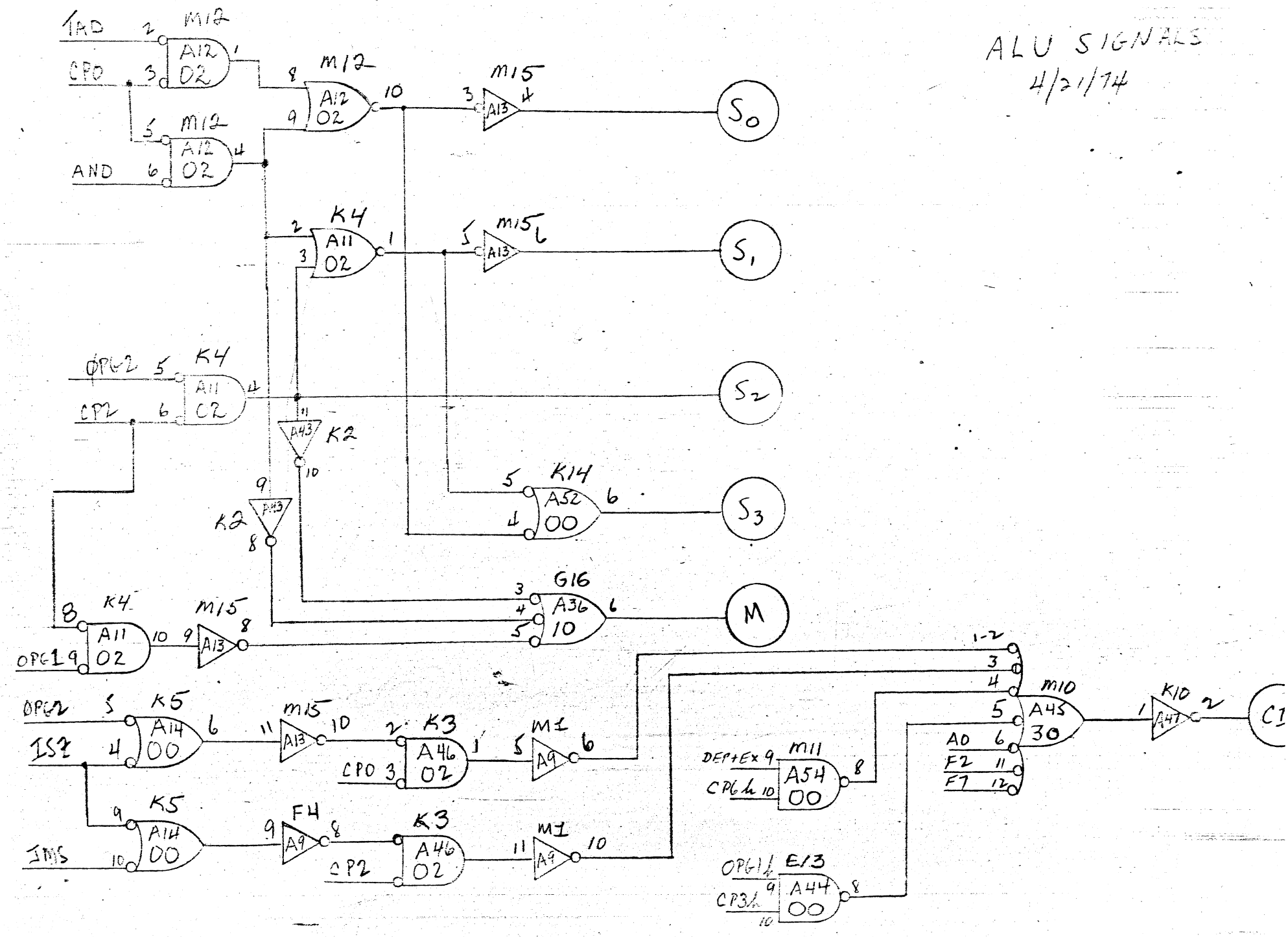


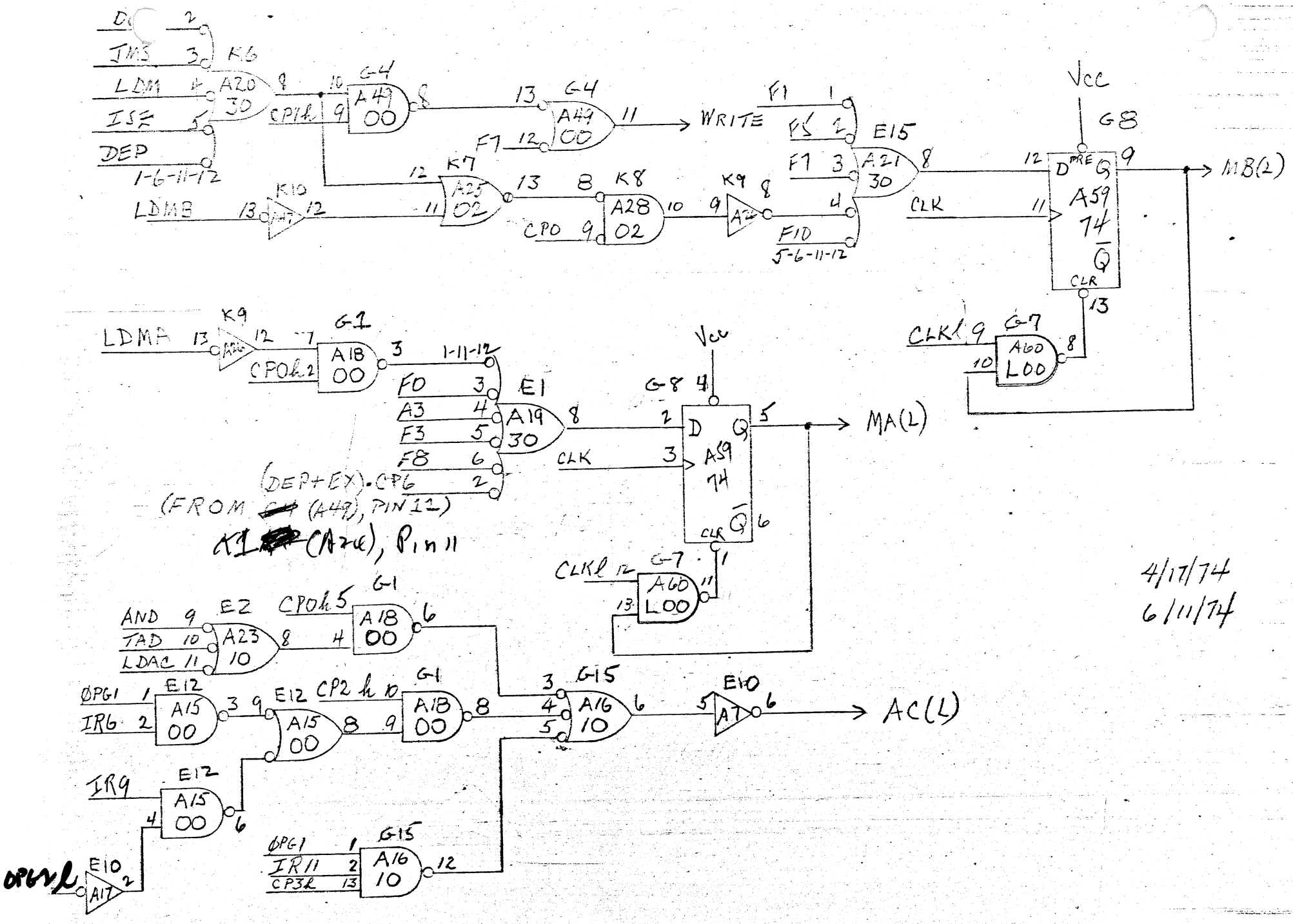

CONTP
L8
CP7h
B47
9024
CLK
CLR
PR
Vcc
A0
FORCE OP CODE TO 4 DURING INTERRUPT
L6
IR2
IR1
IR0
B13
157
STROBE
AND
TAD
ISZ
DCA
JMS
JMP
IOT
MIC
B14
42
L5
M2
A93
02
IR3
OPG1h
M4
A9
OPG1l
M15
A13
K5
A14
00
OPG2
SWONMAND
B8
H13
CP7l
DISABLE IR DURING MANUAL
3/11/74
4/20/74
6/13/74

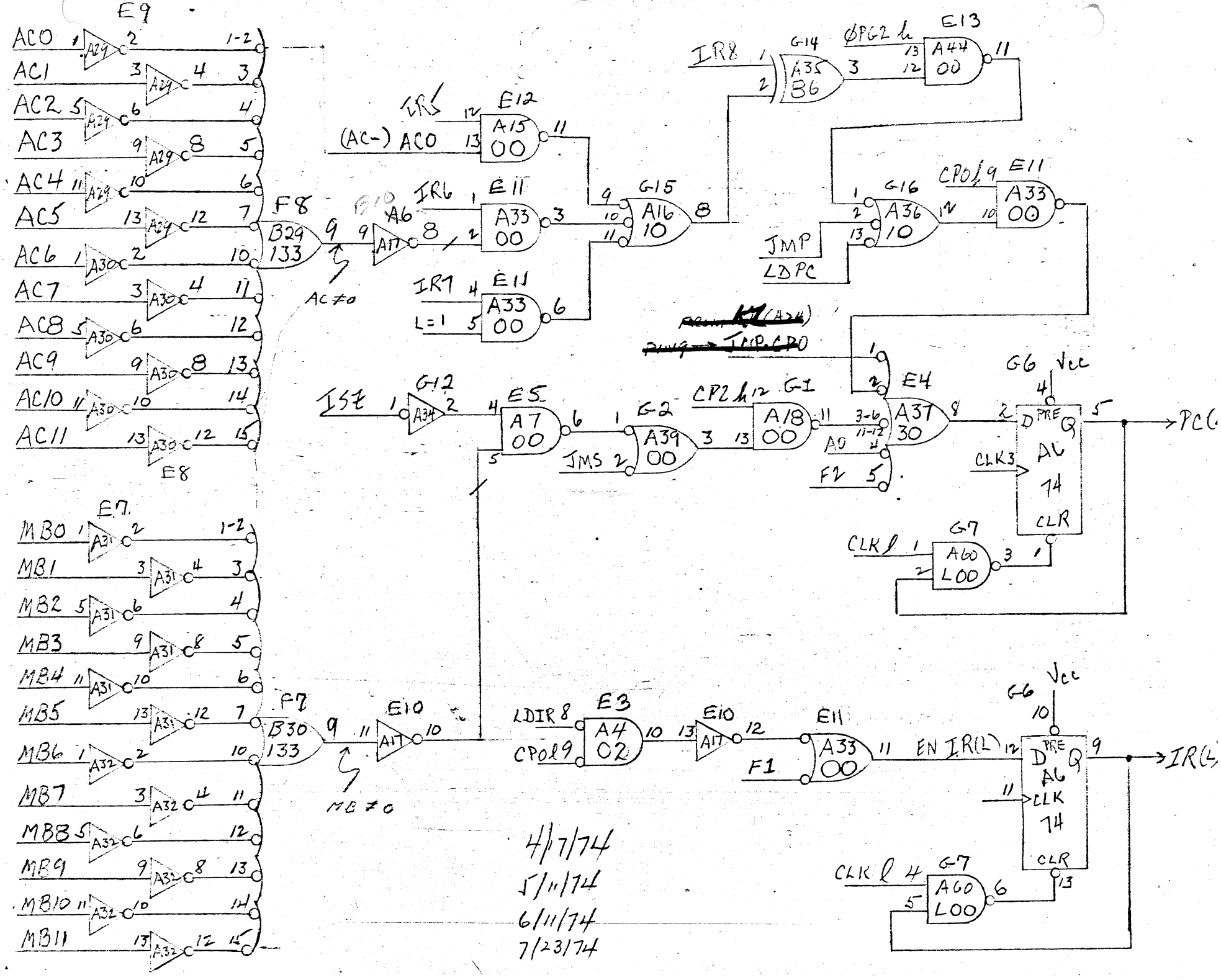


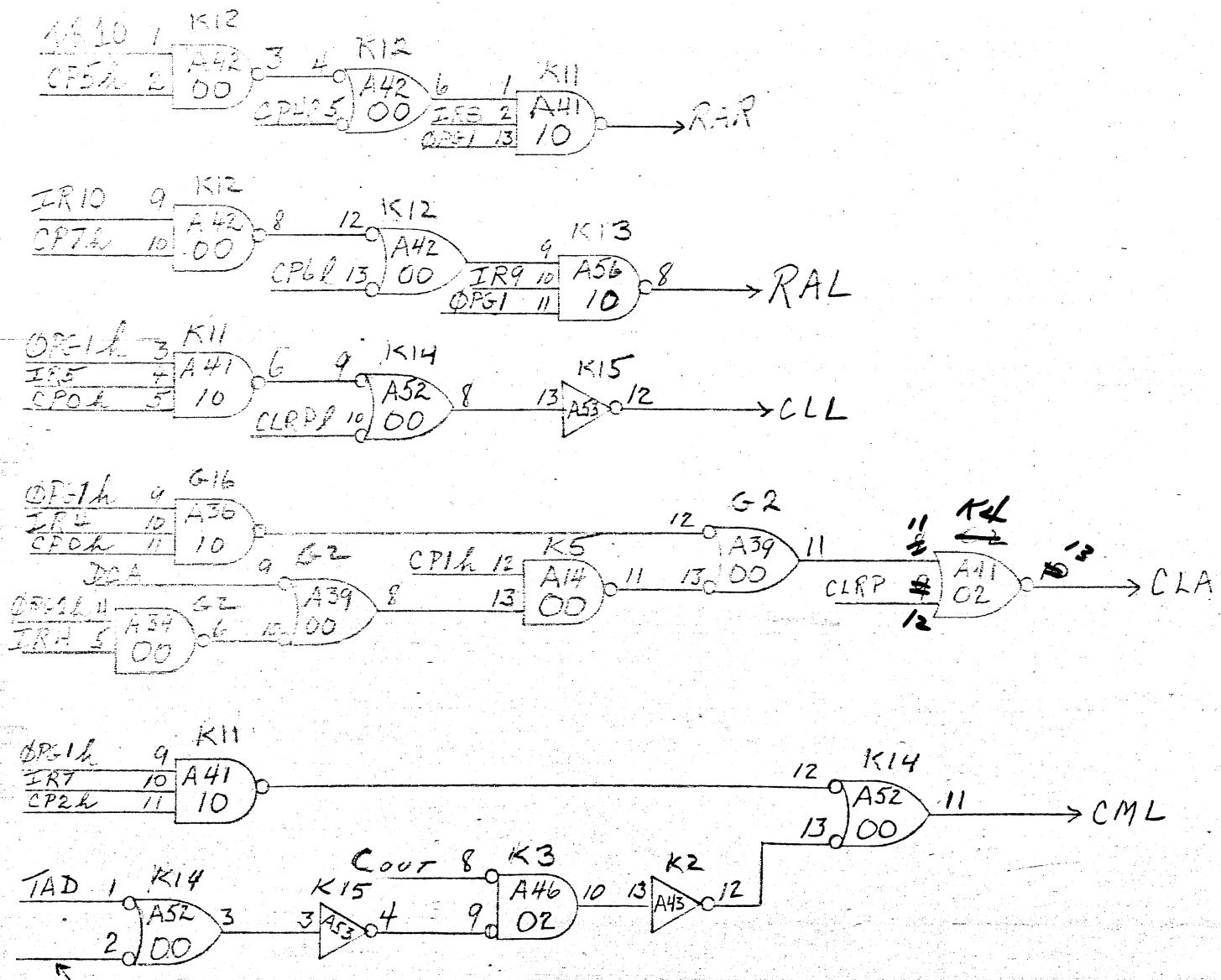
MUX SIGNALS
4/21/74
7/23/74
10/4/74

ALU SIGNALS
4/21/74

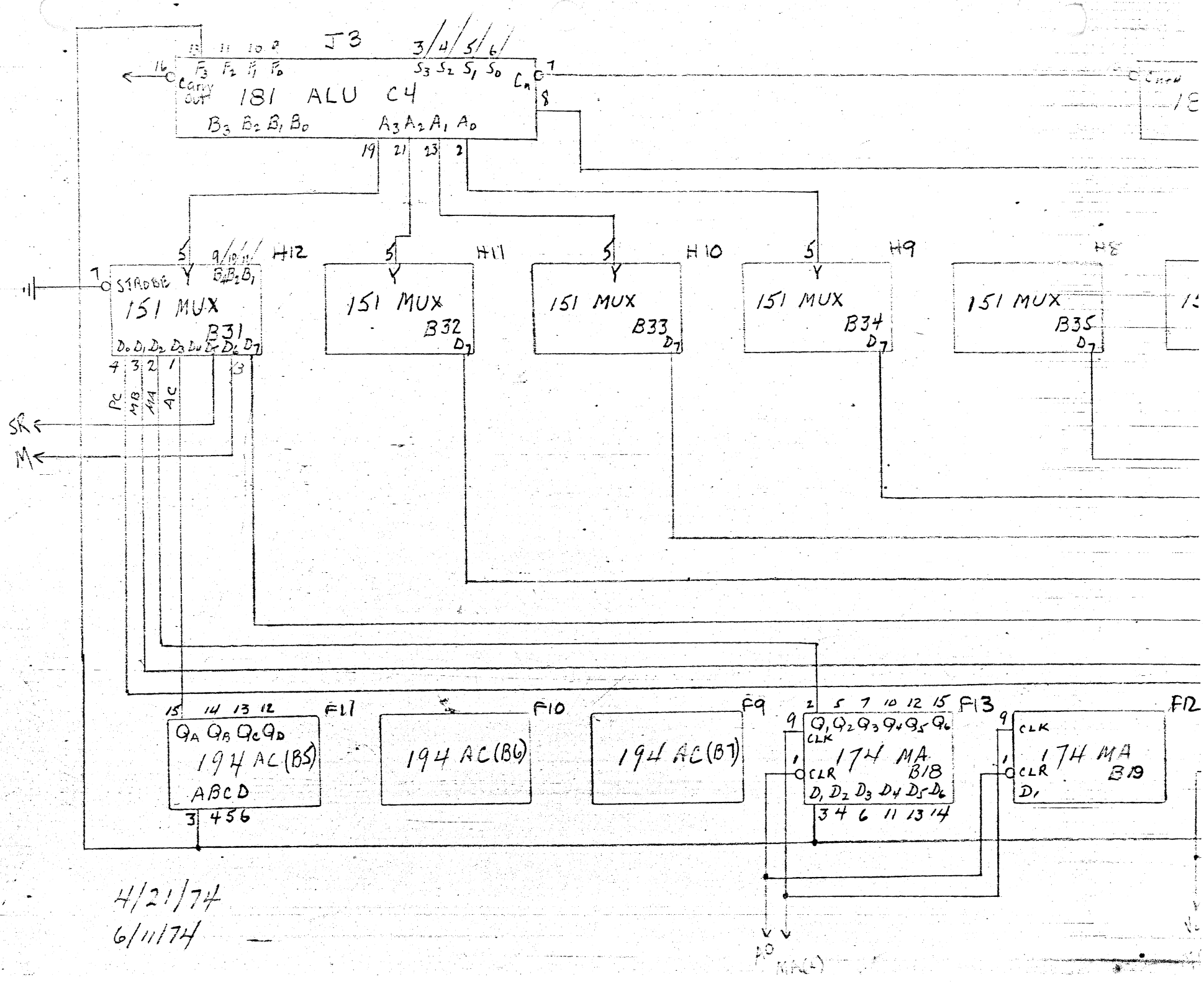


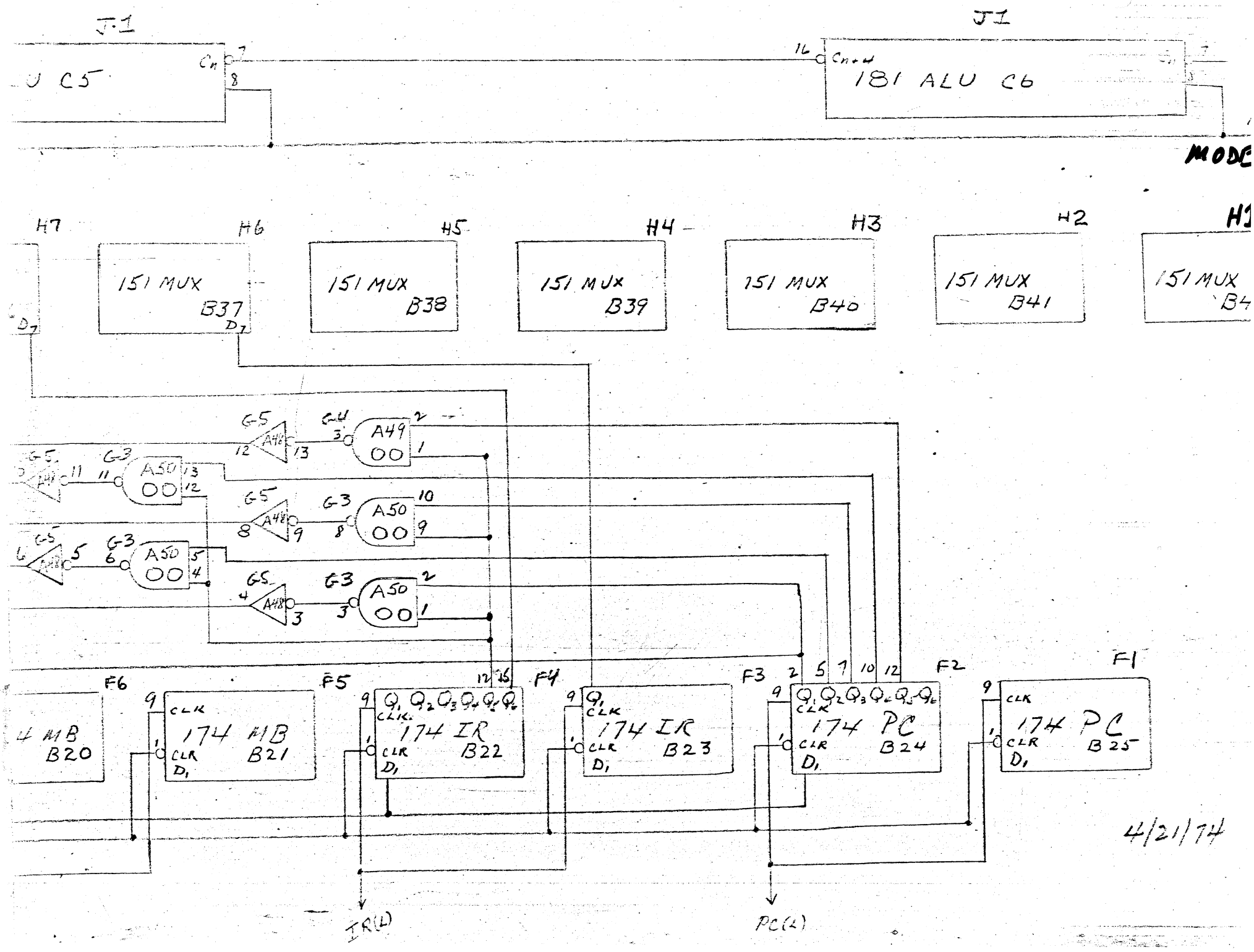

DEP
1-6-11-12
LDMB
K6
A20
30
CP1h
G4
A49
00
WRITE
F7
K7
A25
02
CP0
K8
A28
02
K9
F1
F5
E15
A21
30
F10
5-6-11-12
Vcc
G8
PRE
D
Q
A59
74
CLR
MB(L)
CLKl
G7
A60
L00
LDMA
CP0h
G1
A18
00
F0
A3
F3
F8
E1
A19
30
(DEP+EX)·CP6
(FROM (A49), PIN 12)
K1 (A26), Pin 11
MA(L)
AND
TAD
LDAC
E2
A23
10
CP0h
ØPG1
IR6
E12
A15
00
CP2h
IR9
IR11
CP3h
G15
A16
10
E10
A17
AC(L)
4/17/74
6/11/74


E9
AC0
AC1
AC2
AC3
AC4
AC5
AC6
AC7
AC8
AC9
AC10
AC11
A29
A30
E8
F8
B29
133
AC≠0
E7
MB0
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MB9
MB10
MB11
A31
A32
F7
B30
133
MB≠0
E10
A17
E12
A15
00
(AC-)
IR5
E11
A33
00
IR6
A6
IR7
L=1
G15
A16
10
IR8
G14
A35
86
ØPG2 h
E13
A44
00
G16
A36
10
JMP
LDPC
CP0 l 9
E11
A33
00
IS7
G12
A34
E5
A7
00
JMS
G2
A39
00
CP2 h
G1
A18
00
E4
A37
30
AO
F2
G6
Vcc
PRE
D
Q
AC
74
CLR
CLK3
PC(
G7
A60
L00
CLK l
LDIR
CP0 l 9
E3
A4
02
F1
EN IR(L)
IR(L)
CLK
4/7/74
5/11/74
6/11/74
7/23/74

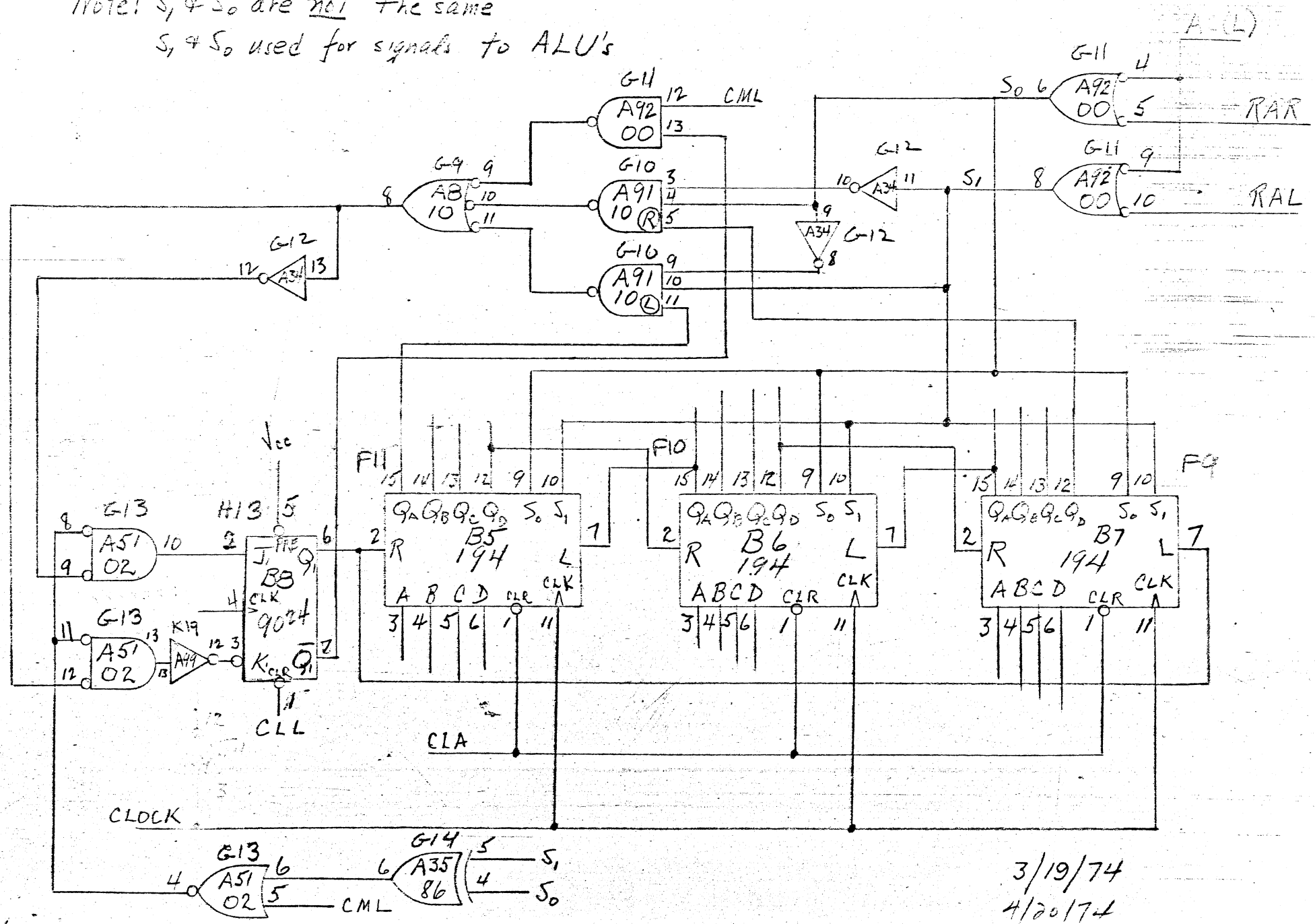


3/19/74
6/11/74
6/18/74


J3
181 ALU C4
Carry out
F_3 F_2 F_1 F_0
S_3 S_2 S_1 S_0
C_n
B_3 B_2 B_1 B_0
A_3 A_2 A_1 A_0
H12
STROBE
151 MUX
B31
D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7
PC
MB
MA
AC
SR
M
H11
151 MUX
B32
H10
151 MUX
B33
H9
151 MUX
B34
H8
151 MUX
B35
F11
Q_A Q_B Q_C Q_D
194 AC(B5)
ABCD
F10
194 AC(B6)
F9
194 AC(B7)
F13
Q_1 Q_2 Q_3 Q_4 Q_5 Q_6
CLK
CLR
174 MA
B18
D_1 D_2 D_3 D_4 D_5 D_6
F12
CLK
CLR
174 MA
B19
D_1
4/21/74
6/11/74

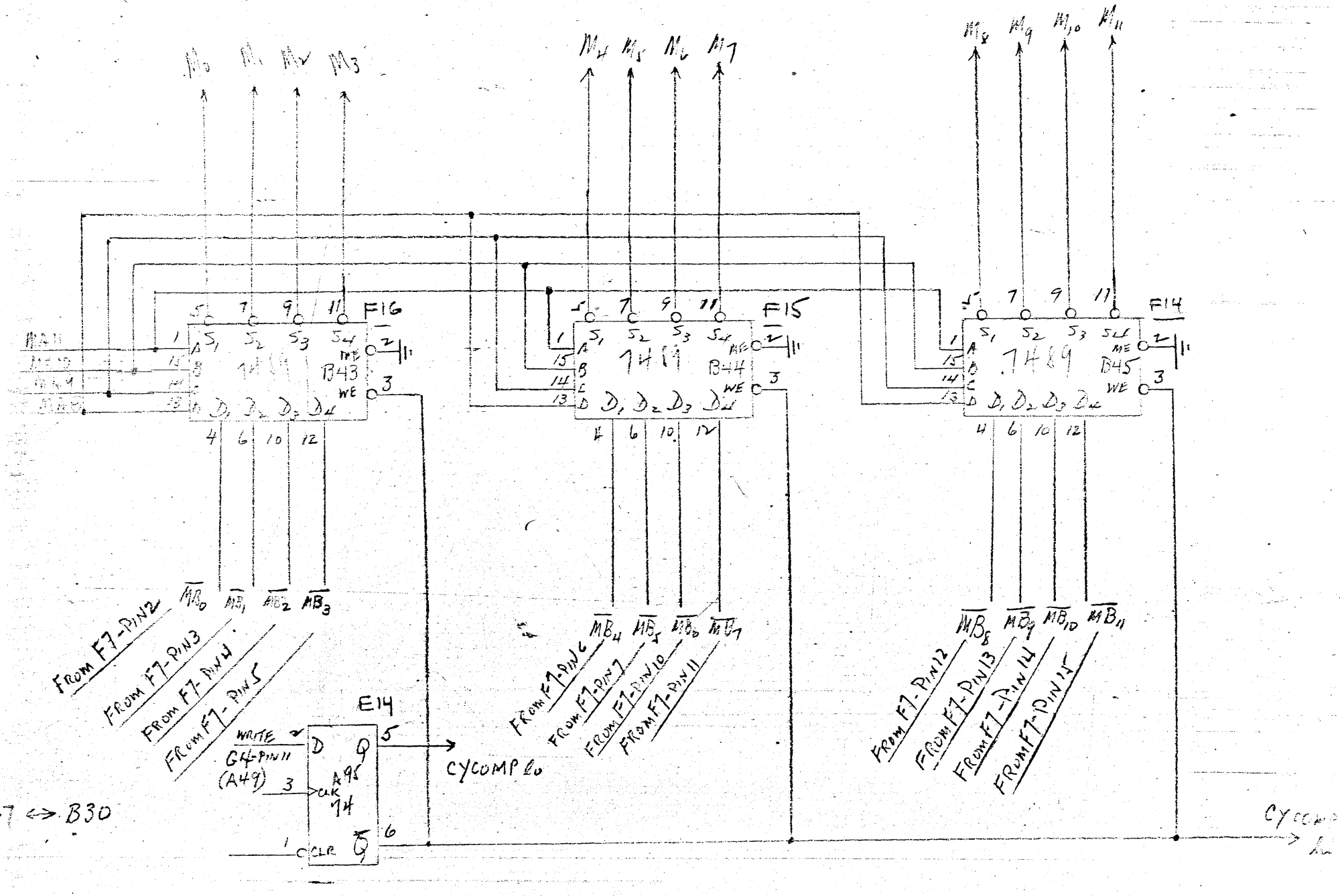

J1
C5
J1
181 ALU C6
MODE
H7
H6
H5
H4
H3
H2
H1
151 MUX B37
151 MUX B38
151 MUX B39
151 MUX B40
151 MUX B41
151 MUX B4
G5
G4
G3
A49
A50
F6
F5
F4
F3
F2
F1
174 MB B20
174 MB B21
174 IR B22
174 IR B23
174 PC B24
174 PC B25
CLK
CLR
IR(L)
PC(L)
4/21/74

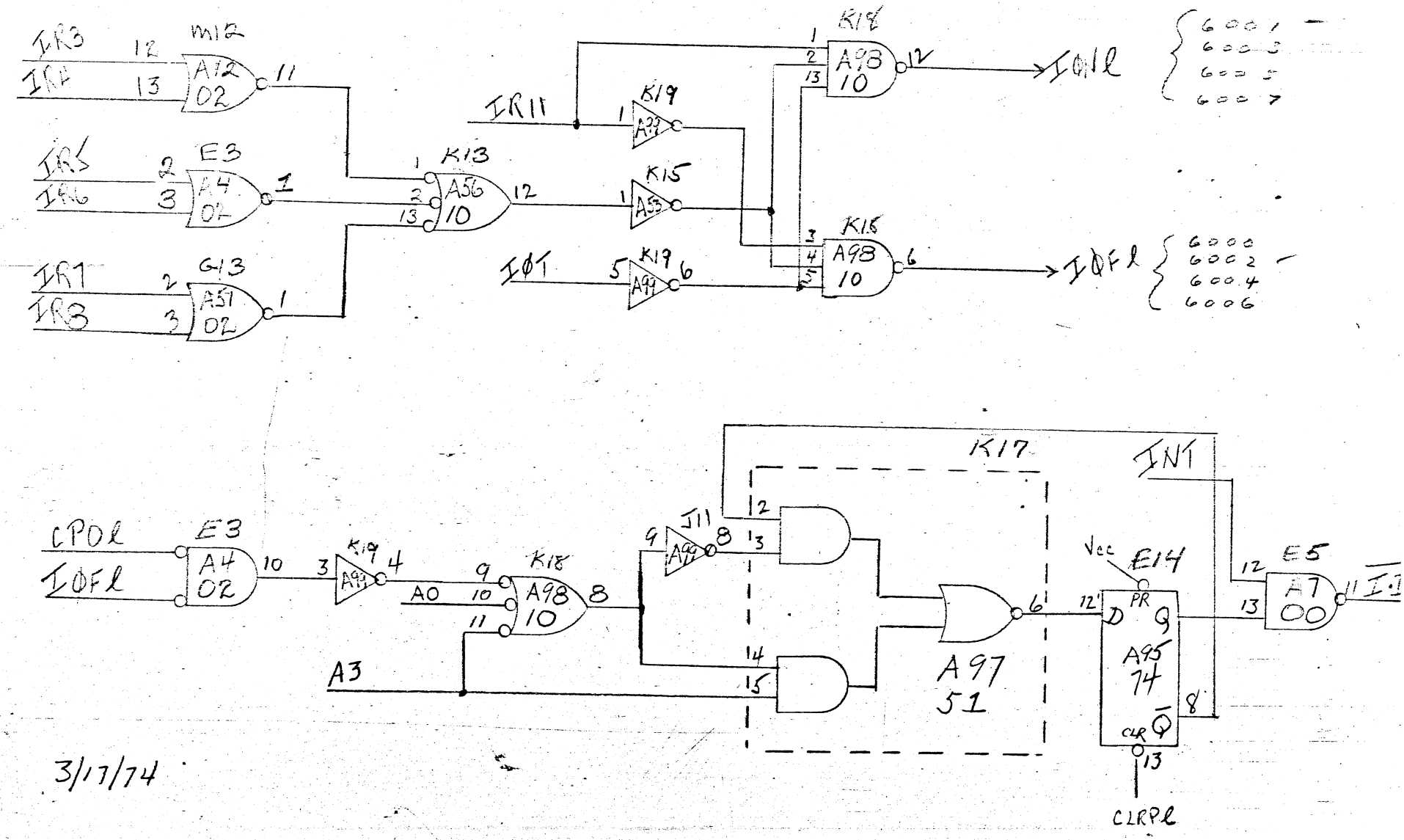
Note: S_1 & S_0 are not the same
S_1 & S_0 used for signals to ALU's



MEMORY
(16 WORDS)

5/11/71
6/11/74




IR3
IR4
M12
A12
02
IR5
IR6
E3
A4
02
IR1
IR3
G13
A51
02
K13
A56
10
IR11
K19
A99
K15
A53
IØT
K19
A99
K18
A98
10
IØFl
K16
A98
10
IØFl
CPOl
IØFl
E3
A4
02
K19
A99
A0
K18
A98
10
A3
J11
A99
K17
A97
51
INT
Vcc
E14
PR
D
Q
A95
74
CLR
Q̄
CLRPl
E5
A7
00

3/17/74